Section IV. THEORY of OPERATION

4.1 Introduction

This section contains a complete functional description of the test set. An explanation of the overall system interface block diagram (figure 4-1) is provided in paragraph 4.2. Explanations of each subassembly (module) detailed block diagrams are provided in paragraph 4.3. Schematic diagrams of subassemblies are provided in Section VI.

4.2 System Block Diagram Description

The TURFTS is a digital, direct sequence, spread spectrum and Continuous Wave RF test set designed to support spacecraft level testing, and prelaunch testing of S-Band Transponders. The TURFTS system uses spread-spectrum techniques to generate a forward uplink (F/L) signal or a CW signal with a phase modulated subcarrier. The TURFTS can receive and demodulate a return downlink (R/L) signal or a CW signal with subcarrier and/or baseband data, and provide the direct control and monitoring necessary to characterize and test the user transponder system performance parameters. TURFTS also offers coherent frequency translation for self-test and calibration. The TURFTS has the capability of providing high accuracy group delay measurements for spread spectrum transponders. The system level simplified block diagram is shown in figure 4-1 illustrating the main components and signal flow. TURFTS consists of a Transmitter, Receiver, RF Distribution and comercially available equipment for monitoring and measuring signal parameters. The time interval counter is used for making group delay measurements for TDRSS user transponders. The scope is used to monitor data and other internal signals to aid in analyzing what is going on within the test set. The spectrum analyzer is used to monitor the front end of the test set as well as IF signals and the transmitted signal.

4.2.1 The TURFTS Computer System

The controls and main indicators for the TURFTS system are in the form of graphical windows in the TURFTS control program. The control program runs on a PC and was developed using National Instruments LabVIEW software. The graphical user interface provides the user with the capabilities of configuring and operating the TURFTS system. The TURFTS control program can be configured for remote or local operation. The Remote operation can be through a serial port or TCP/IP.

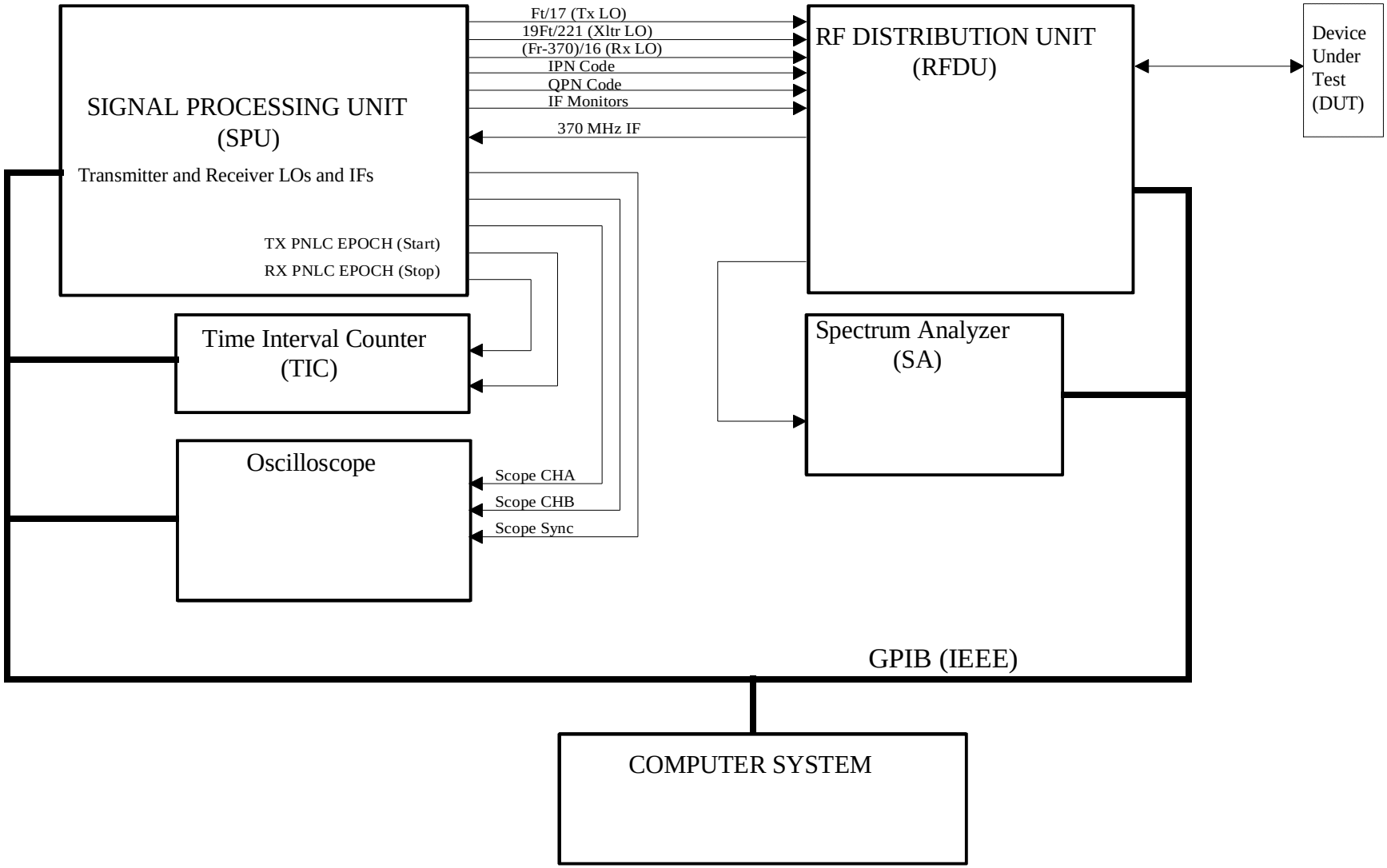

Figure 4-1. Overall system interface simplified block diagram

4.2.2 Signal Processing Unit (SPU)

The SPU is an integral part of both transmitter and receiver functions. Refer to Figure 4-2. All reference frequencies and LOs for the test set are generated in the SPU modules A2 through A4. Through the P1 Control BUS A1 and A7 control the frequencies for acquisition and tracking of the incoming signal.. The SPU modules A5, A6 and A12 will, at the 370 MHz IF, acquire, track, and recover data from an S Band transponder configured in a Spread Spectrum mode or in a CW mode with a PM subcarrier and/or baseband data. Through the P2 Signal BUS the recovered telemetry goes to module A8 for bit synchronization and module A12 for subcarrier acquisition and tracking. The SPU can also provide simulated data for testing purposes as well as several monitor points both RF and digital.

4.2.3 RF Distribution Unit (RFDU)

This assembly contains all of the S-band processing circuitry necessary for maximum signal isolation. One of its function is to facilitate the translator circuitry used to convert the forward link (F/L) S-band signal to the return link (R/L) S-band signal when operating in the self test (XLTR) mode. Second, it functions as an interface unit processing (F/L) and (R/L) S-band signals using a diplexed transmission line between the test set and the Device Under Test or separate transmit and receive lines to the DUT. Third, it houses the RF down converter circuitry to produce the receiver's first IF at 370 MHz and the RF up converter to produce the S-band F/L. The RF Distribution simplified interface block diagram (figure 4-3) illustrates how this drawer functions as an interface between the DUT, the test transmitter, and the test receiver.

Translator Mode (XLTR). An S-band transmitter signal (2025-2120 MHz) produced in the RF Output Module (A9) is routed through a diplexer and then switch S1 to the Translator Module (A4) where a circulator isolates the Transmit signal input and the Receive signal output. The transmit signal is mixed with the translator local oscillator (XLTR LO, 174.1-182.26 MHz) from the Transmitter Frequency Synthesizer Module located in the SPU (A4A3). A bandpass filter (BPF) is then used to isolate the desired first sum mixer product of 2200-2300 MHz. The output receive signal from the filter goes through the circulator and is routed back through switch S1 and the diplexer to the receiver's coarse attenuator, a BPF, and the Down Converter Module. The down converter consists of a 20 dB gain low noise amplifier (LNA), a double balanced mixer, a BPF and a wideband amplifier with 47 dB gain. The 2200-2300 MHz signal is mixed with 1830-1930 MHz to provide an IF signal at 370 MHz which is sent to the SPU Tracking IF Module A4A5).

Transponder Mode (XPNDR). By utilizing a diplexer, a single transmission line can be used for both the forward link (F/L) and return link (R/L) signals. The F/L (2025-2120 MHz) is routed through the diplexer and switch S1 to the transponder under test. The R/L from the transponder is routed through switch S1 and the diplexer to the down converter circuitry as described in the previous paragraph. The diplexer can be bypassed utilizing RF switches S2 and S3 for independent transmit and receive capabilities.

WARNING

The level from the transponder at switch S1 or S3 should <u>not</u> exceed +10 dBm.

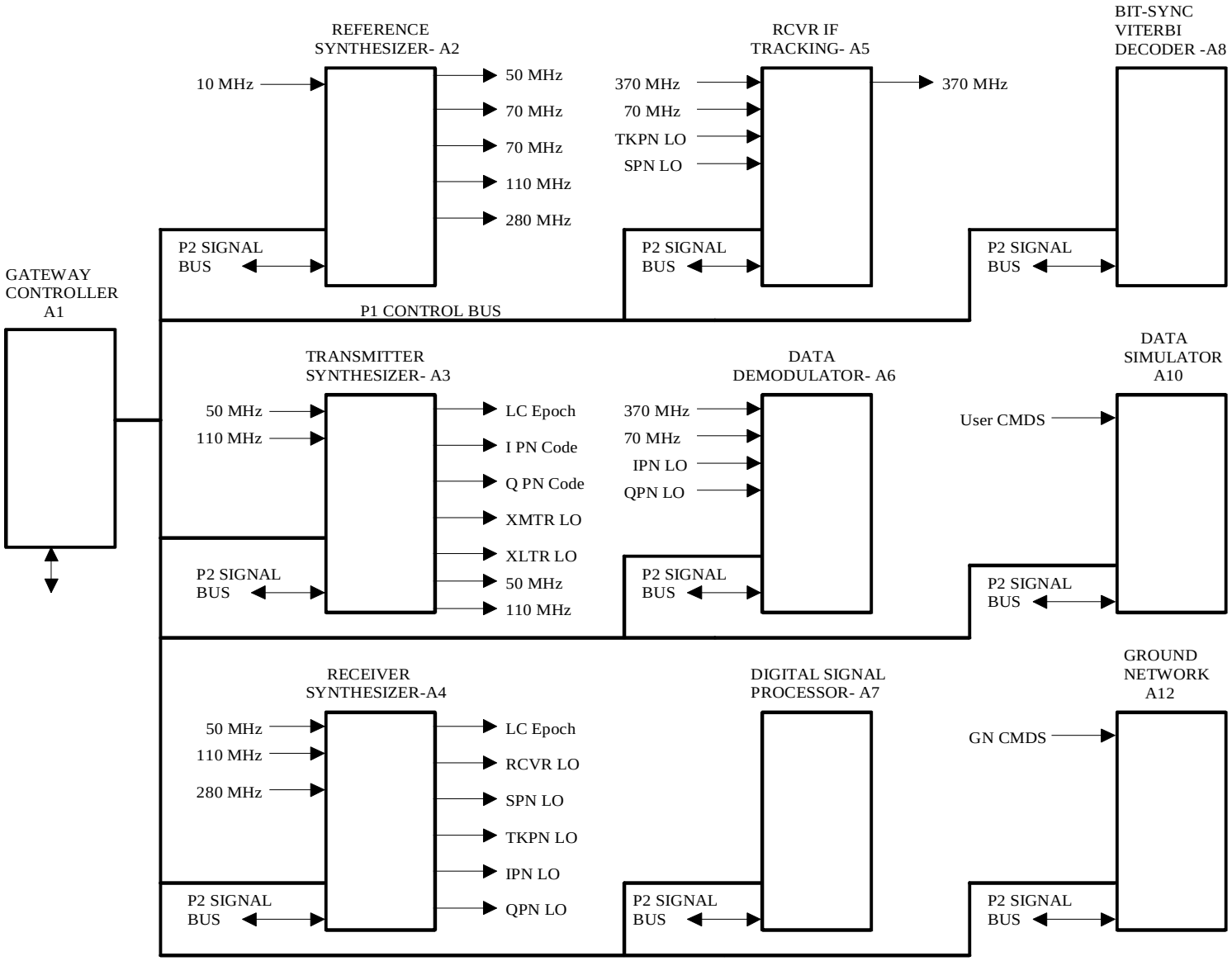

Figure 4-2. SPU Simplified Block Diagram

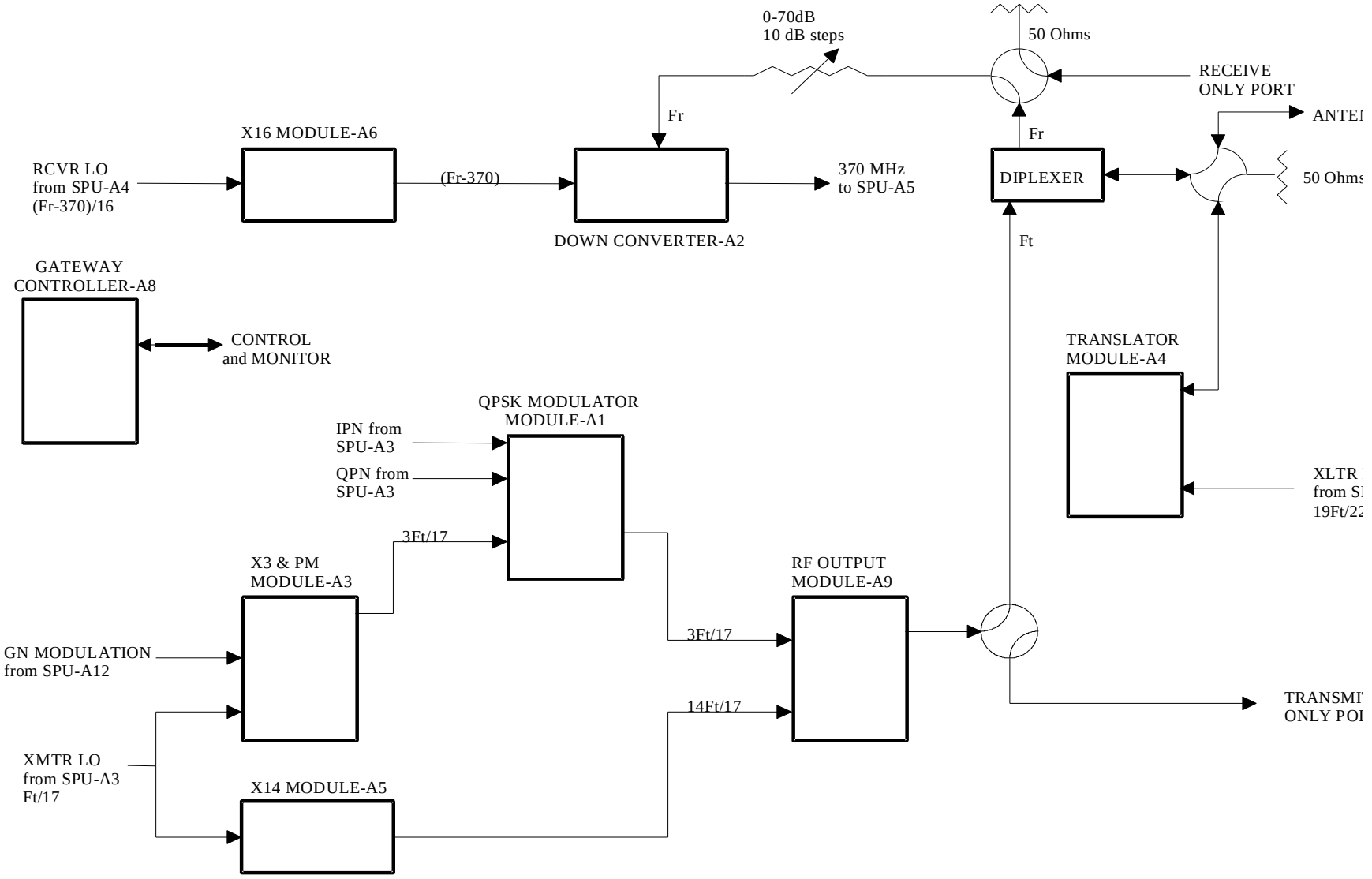

Figure 4-3. RFDU Simplified Block Diagram

4.3 Detailed Description of the Subassemblies used in the RFDU

4.3.1 QPSK Modulator (A3A1)

In the following discussion refer to Figure 4-4 and Schematic 6-xx. The RF input (3Ft/17) comes from the X3 Multiplier & PM module A3A3 and is split by a 90 degree hybrid to provide the in-phase and quadrature-phase signals. The in-phase signal level and quadrature phase signal can be adjusted using a voltage controlled attenuator set at time of alignment by R3 and R4. This adjustment is used to match the levels between the in phase channel and the quadrature phase channel. Both channels go through active phase shifters where the quadrature channel is fixed and the in phase channel is adjusted at time of alignment by R9. This adjustment is to fine tune the quadrature between the two channels. Each channel is then bi-phase modulated by the respective psuedorandom codes IPN to the in phase channel and QPN to the quadrature channel. The two signal levels are then independently set using digital attenuators to establish the power ratio between the two channels. Control of these attenuators are through the RFDU gateway controller - A8. After the signal level ratios are set, the signals are combined, amplified and transmitted to the RFDU RF Output Module - A9 for upconversion to the S-Band signal. A directional coupler provides a sample of the output to a threshold detector that determines whether there is a fault due to a level drop in the signal. This monitor is returned the the RFDU Gateway controller - A8 for processing.

4.3.2 Down Converter (A3A2)

In the following discussion refer to Figure 4-5 and Schematic 6-xx. The S-Band received signal (2200 - 2300 MHz) is sent to the down converter through the receiver step attenuator and bandpass filter. The signal is amplified by a low noise amplifier and mixed with a local oscillator (Fr - 370) which comes from the X16 Multiplier (A3A6). The lower side band (370 MHz) is filtered and amplified to provide the first receiver IF to the SPU Receiver IF Tracking Module (A4A5). The signal is also 10 dB coupled for monitoring on the spectrum analyzer.

4.3.3 X3 Multiplier and Phase Modulator (A3A3)

In the following discussion refer to Figure 4-6 and Schematic 6-xx. The RF input (Ft/17), which comes from the SPU Transmitter Frequency Synthesizer Module (A4A3) goes through a switch network U11 and U12 that will either pass the signal straight through to be multiplied or route the signal through a linear modulator that adds the combined modulation from the SPU GN module (A4A12) and is then multiplied. U13 and U17 provide the proper biasing of the modulation input and is adjusted at test to provide maximum carrier suppresion based on an input level of +10 dBm. The times three multiplier circuit consists of U1 through U7. The signal is divided with one output multiplied by two and mixed with the other output to provide the times three signal. The resultant signal is filtered and amplified to provide the input signal to the QPSK Modulator. The times three signal is also coupled and RF detected to provide a fixed voltage for fault monitoring. This monitor is returned the the RFDU Gateway controller - A8 for processing.

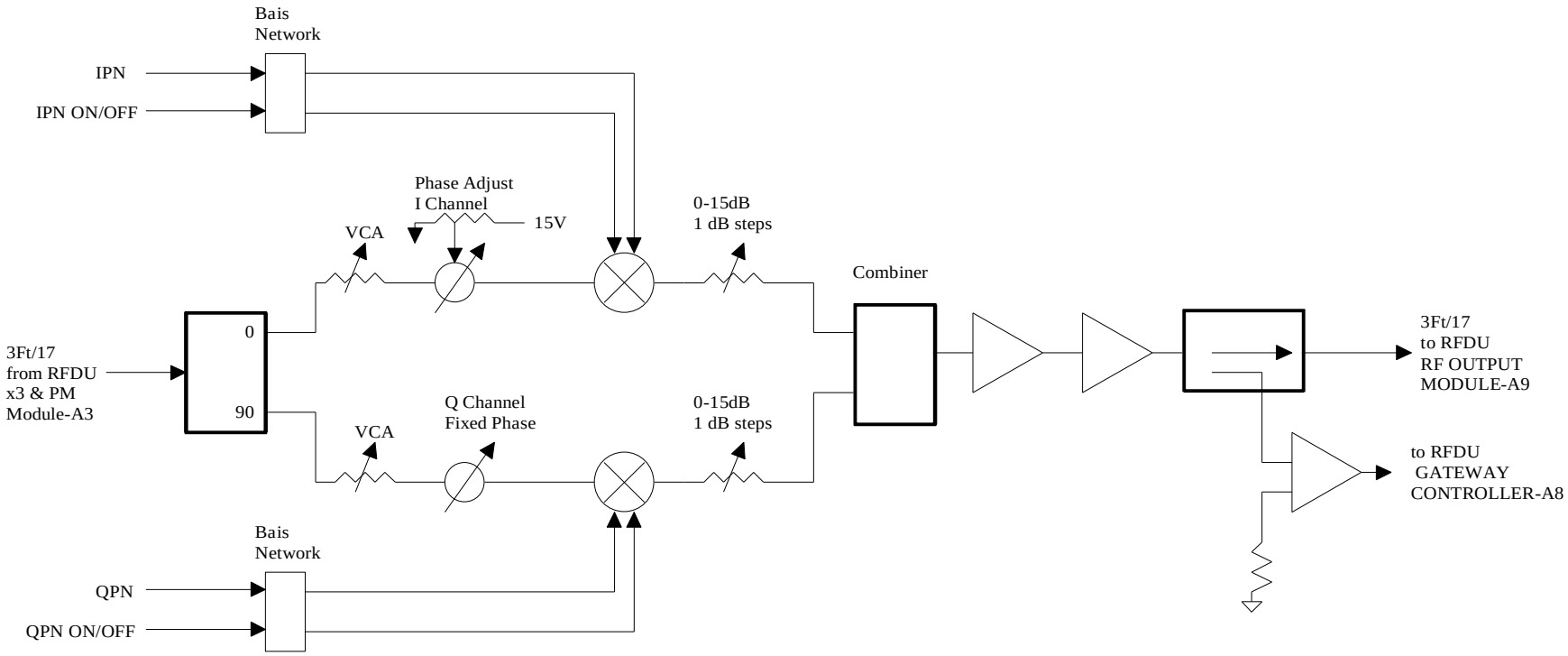

Figure 4-4. QPSK Modulator Simplified Block Diagram

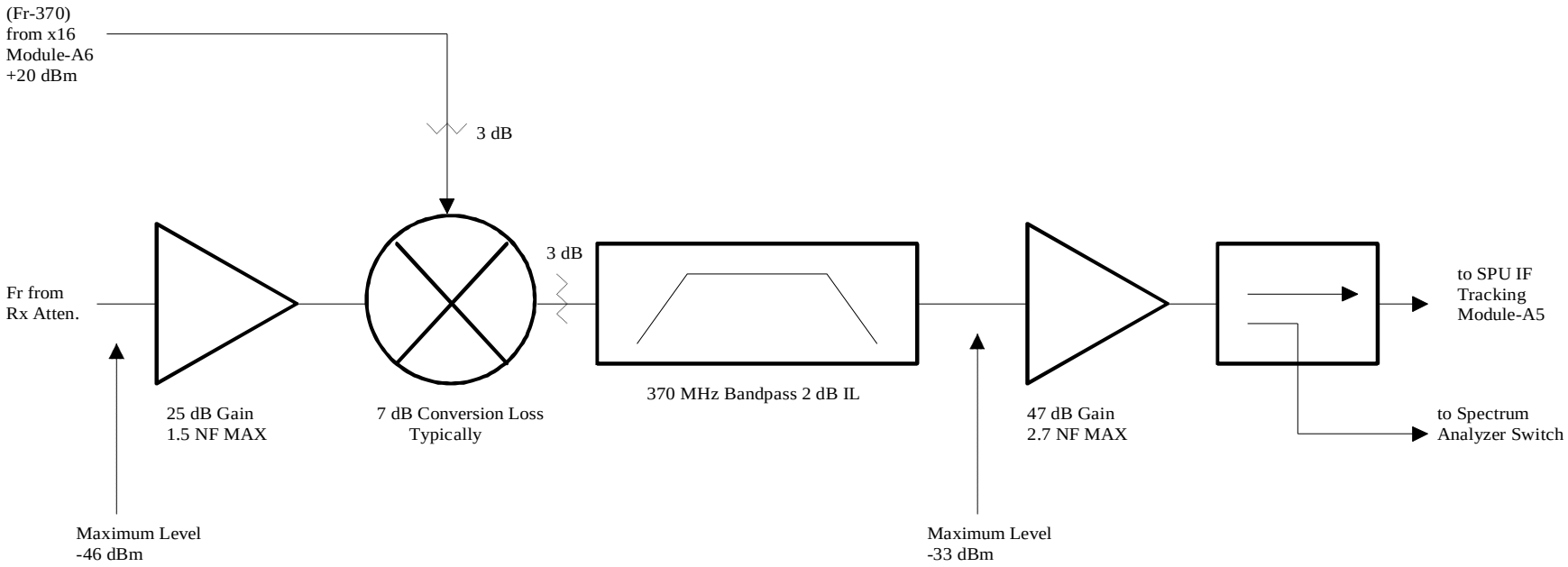

Figure 4-5. Down Converter Assembly Simplified Block Diagram

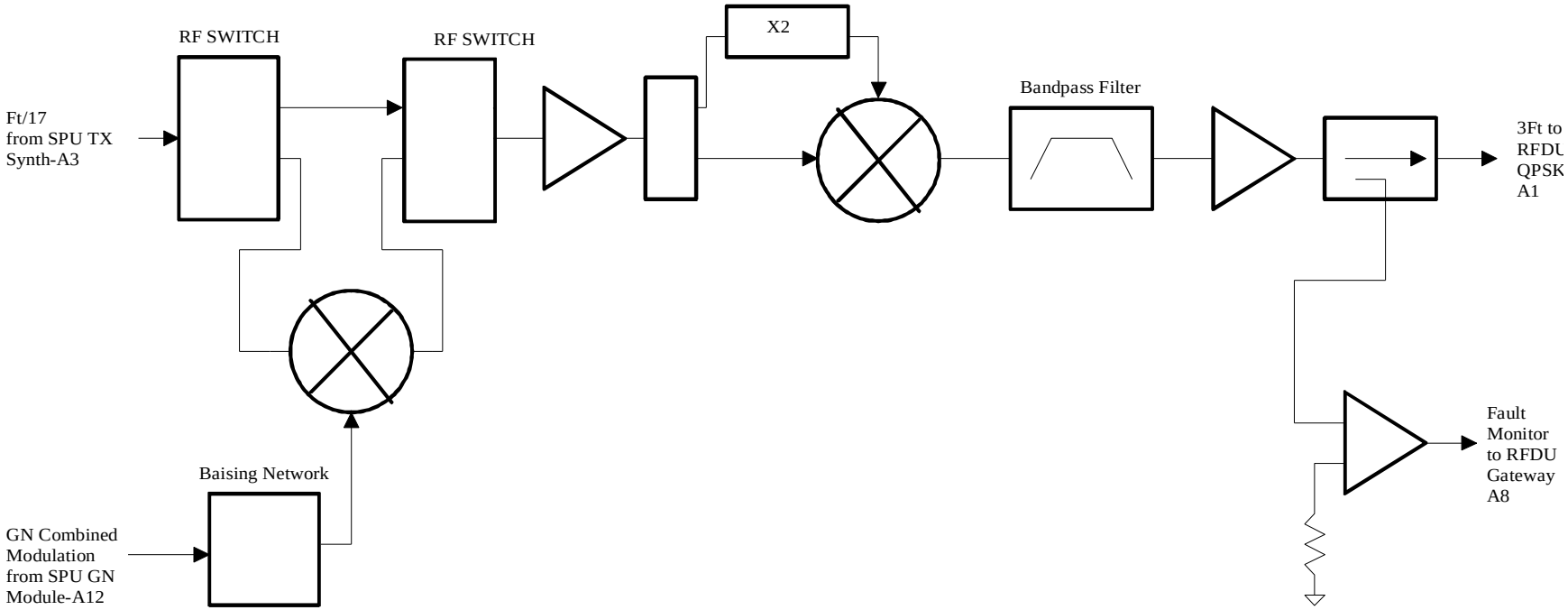

Figure 4-6. X3 and PM Module Simplified Block Diagram

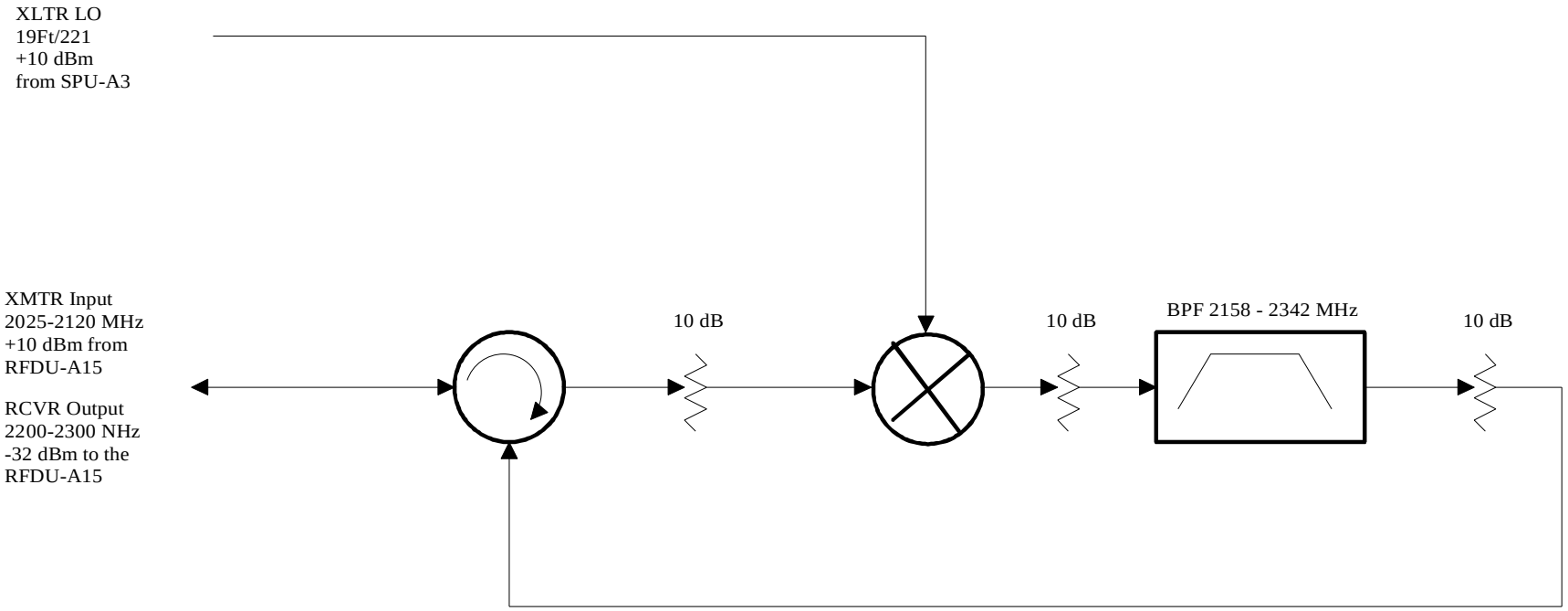

Figure 4-7. Translator Module Simplfied Block Diagram

4.3.4 Frequency Translator (A3A4)

In the following discussion refer to Figure 4-7 and Schematic 6-xx. The Translator module receives 19Ft/221 (XLTRLO) from the Transmitter Frequency Synthesizer Module (A4A3). This is mixed with the S-Band Transmit signal Ft (2025 - 2120 MHz) from the RF Output Module (A3A9) and bandpass filtered to provide the R/L signal Fr (2200 - 2300 MHz) when the test set is operating in the self test mode. A circulator is used to isolate Ft from Fr since they both share the same RF Port, J2. The translated conversion loss is approximately 42 dB and the two way delay is approximately 15 nsecs.

4.3.5 X14 Multiplier (A3A5)

The x14 Module is a Commercial Of The Shelf (COTS) module and no block diagram is shown. The input is Ft/17 (XMTRLO) from the Transmitter Frequency Synthesizer Module A4A3. The output (14Ft/17) goes to the RF Output Module (A3A9) where it is mixed with (3Ft/17) to prove the transmit signal. A lock indicator is provided for monitoring at the System Controller through the RFDU Gateway controller (A3A8).

4.3.6 X16 Multiplier (A3A6)

The x16 Module is a Commercial Of The Shelf (COTS) module and no block diagram is shown. The input is ((Fr-370/16) (RCVRLO) from the Receiver Frequency Synthesizer Module (A4A4). The output (Fr-370) goes to the Down Converter Module (A3A2) where the S-Band received signal is converted to 370 MHz. A lock indicator is provided for monitoring at the System Controller through the RFDU Gateway Contoller (A3A8).

4.3.7 Gateway Controller and Driver Board (A3A8)

In the following discussion refer to Figure 4-8 and Schematic 6-xx. This board provides the interface between the System Controller and the RF Distribution Unit (RFDU) by use of a GPIB microprocessor chip (TMS9914) and controls and receives status from the RFDU modules by use of a Motorola MC68332 microprocessor chip. The Gateway Controller board sets both receiver and transmitter attenuators, configures the RF switches for different RF monitoring and signal flow, sets the power ratio between the I and Q channels, configures the transmitter for QPSK, BPSK, or PM mode, sets the output of the leveling loop, and controls the RF on/off switch.

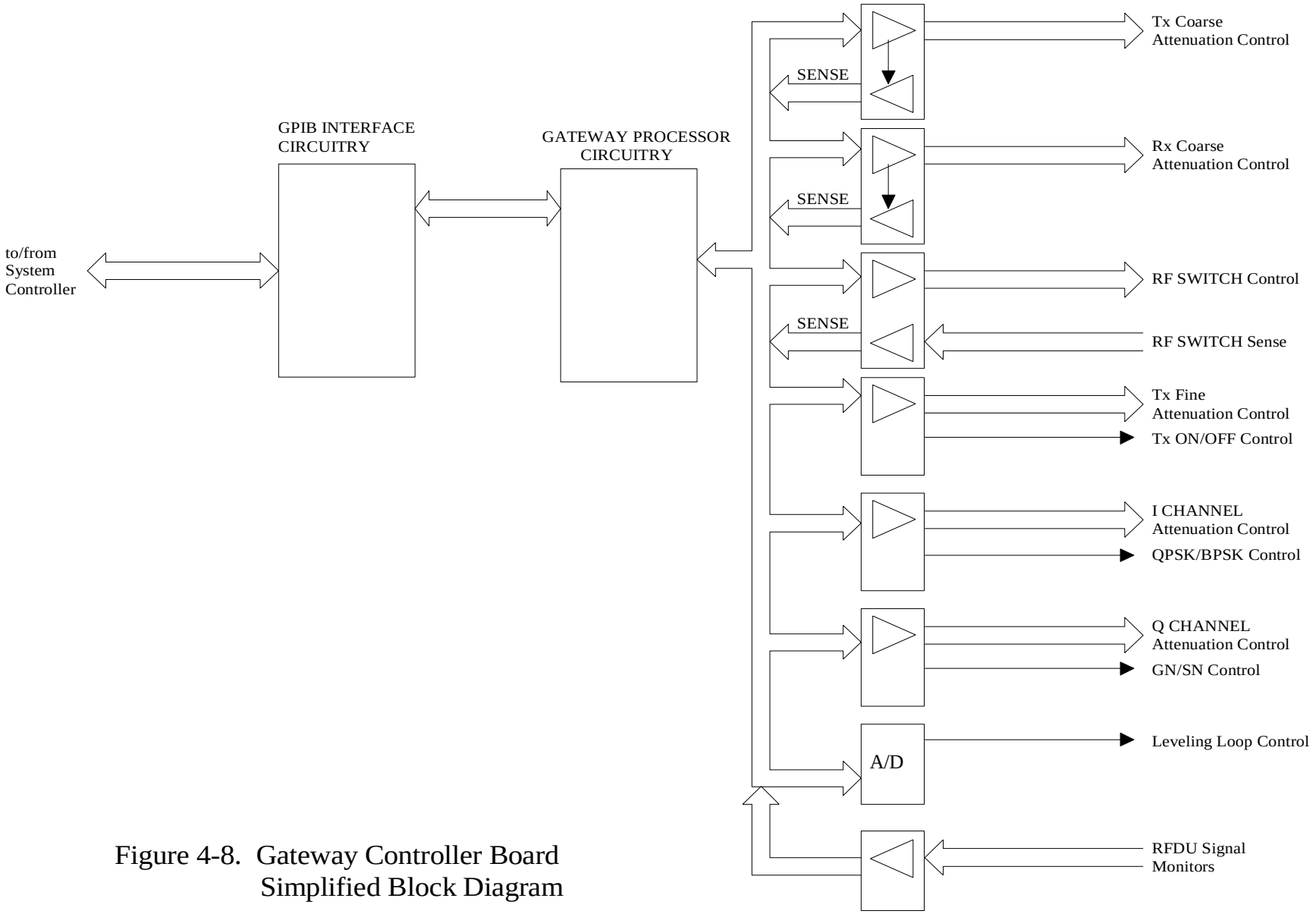

Figure 4-8. Gateway Controller Board Simplified Block Diagram

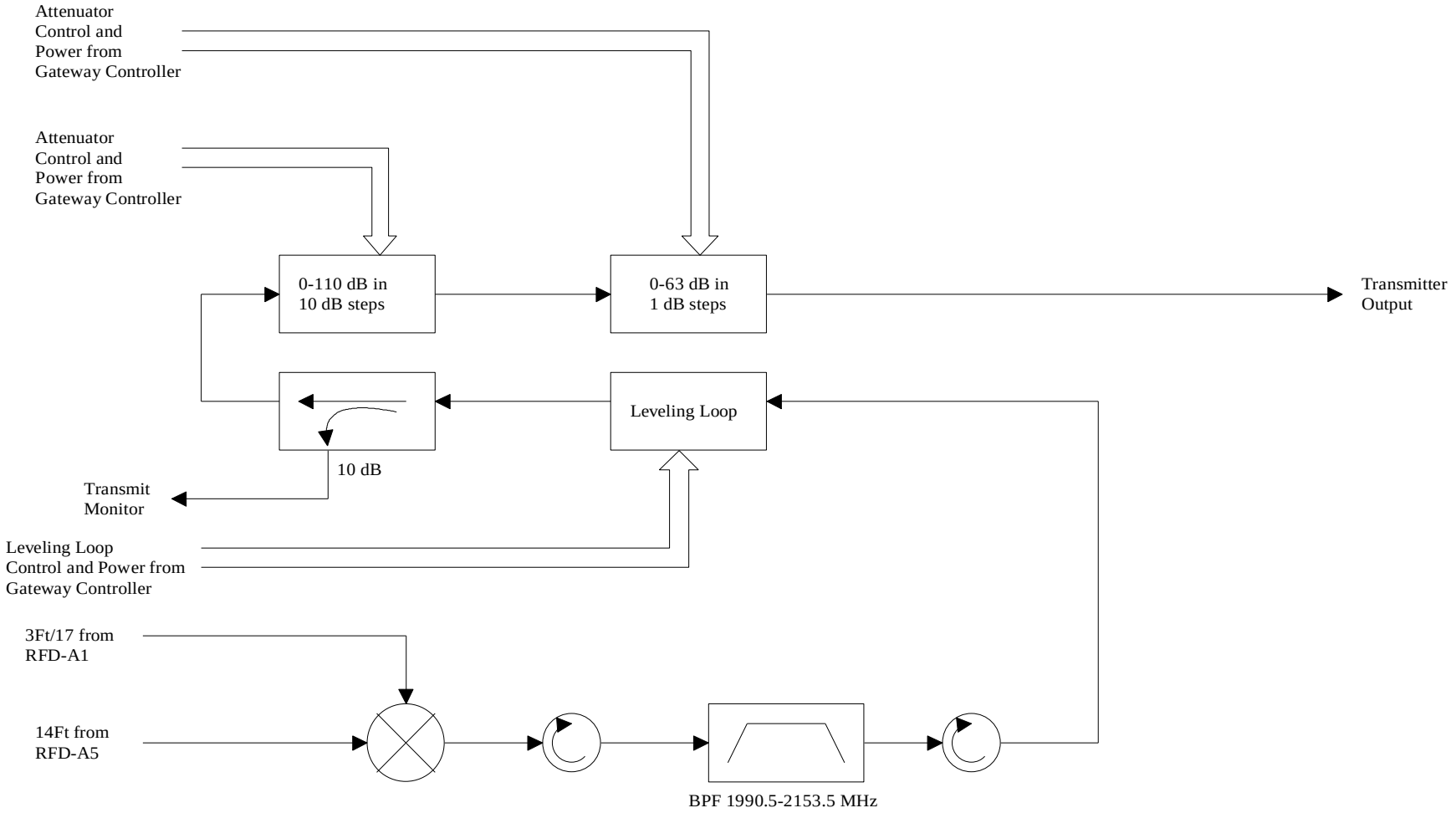

Figure 4-9. RF Output Module Simplified Block Diagram

4.3.8 RF Output Module (A3A9)

In the following discussion refer to Figure 4-9 and Schematic 6-xx. The (14Ft/17) from the X14 Module A3A5 and (3Ft/17) from the QPSK Module A3A1 are mixed and bandpass filtered to provide the transmitter frequency Ft (2025 - 2120 MHz). The signal goes to an auto leveling loop that provides amplification and a level set range from 0 to 10 dB. The level is controlled by the System Controller through the RFD Gateway Controller Board A3A8 by providing a dc voltage from 0 to 5 Volts from an 8-bit D/A converter. The output of the leveling loop is coupled through a 10 dB coupler to provide a transmit monitor port to the spectrum analyzer and is also routed through two programmable attenuators. One attenuator provides 0-63 dB of attenuation in dB steps while the second attenuator provides0-110 dB of attenuation in 10 dB steps. Both attenuators are controlled from the System Controller through the Gateway Controller Board. The final output goes to the RF switch S2 where it is either switched to the transmit port of the diplexer or directly out to the Device Under Test (DUT).

4.4 Detailed Description of the Subassemblies used in the SPU

4.4.1 Gateway Controller (A4A1)

In the following discussion refer to Figure 4-10 and Schematic 6-xx. This board provides the interface between the System Controller and the Signal Processing Unit (SPU) by use of a GPIB microprocessor chip (TMS9914) and controls and receives status from the SPU modules by use of a Motorola MC68332 microprocessor chip.

4.4.2 Reference Frequency Source (A4A2)

In the following discussion refer to Figure 4-11 and Schematic 6-xx. This subassembly provides all the reference frequencies for the test set. The 10 MHz Oven Crystal oscillator used as a reference for the Test Set is located in the RF Distribution Unit Subsystem. This signal inputs at J4 on the front panel of A2. The power divider U1 spits the 10 Mhz into two paths. One path is attenuated by U2 and amplified by U3 before going through a 10 dB coupler U4. The uncoupled port is power divided by U5 to provide three 10 MHz references for the commercial test equipment used within the test set. Reference 1 is supplied to a Spectrum Analyzer; Reference 2 is supplied to a Time Interval Counter and Reference 3 is a spare that goes to the rack's rear interface panel. The coupled port is sent to an RF Threshold detector U6 for fault monitoring. If the level drops below TBD dBm the output of the detector will go TTL low and the output of the 8-Input Nandgate U43 will illuminate the fault light on the front panel. The TTL output from U6 is also transmitted to the System Controller over the VME bus to a fault monitoring screen. The second 10 Mhz path from U1 goes to an ultrafast TTL Comparator U36 where it is converted to a 10 Mhz TTL clock. R10 is a 10 Kohms trim potentiometer used to adjust the symmetry of the clock signal. Odd harmonics are generated by U12 and U18 from the fundamental 10 Mhz clock. The 11th harmonic is filtered and amplified to provide the 110 Mhz reference which is used by the Transmitter and Receiver synthesizer modules A3 and A4. The coupled port of U16 is sent to an RF Threshold detector U17 for fault monitoring. If the level drops below TBD dBm the output of the detector will go TTL low and the output of the 8-Input Nandgate U43 will illuminate the fault light on the front panel. The TTL output from U17 is also transmitted to the System Controller over the VME bus to a fault monitoring screen.

The 5th harmonic is filtered and amplified to provide the 50 Mhz reference which is used by the Transmitter and Receiver synthesizer modules A3 and A4. The coupled port of U10 is sent to an RF Threshold detector U11 for fault monitoring. If the level drops below TBD dBm the output of the detector will go TTL low and the output of the 8-Input Nandgate U43 will illuminate the fault light on the front panel. The TTL output from U10 is also transmitted to the System Controller over the VME bus to a fault monitoring screen. The 7th harmonic is filtered, amplified and divided into four paths. Two paths provide the 70 Mhz reference for IF Tracking Module A5 and the Demodulator Module A6. The third path goes to a Threshold detector U23 for fault monitoring. If the level drops below TBD dBm the output of the detector will go TTL low and the output of the 8-Input Nandgate U43 will illuminate the fault light on the front panel. The TTL output from U23 is also transmitted to the System Controller over the VME bus to a fault monitoring screen. The fourth path is multiplied by 4, amplified and filtered to provide the280 Mhz reference which is used by the Receiver synthesizer module A4. The coupled port of U34 is sent to an RF Threshold detector U35 for fault monitoring. If the level drops below TBD dBm the output of the detector will go TTL low and the output of the 8-Input Nandgate U43 will illuminate the fault light on the front panel. The TTL output from U35 is also transmitted to the System Controller over the VME BUS to a fault monitoring screen.

4.4.3 Transmitter Frequency Synthesizer Module (A4A3)

In the following discussion refer to Figure 4-12 and Schematic 6-xx. This subassembly generates the transmitter's local oscillator (TxLO), the translator's local oscillator (XltrLO), the transmitter's IPN and QPN codes and the Long Code (LC) epoch signal. The 50 Mhz reference from A2 comes in at J5 on the front panel. The power divider U43 splits the reference into two paths. One path goes out J4 on the front panel where it is used in A4 the Receiver Synthesizer Module. The other path goes to U41 an AD9696 uktrafast TTL Comparator which is used to drive the STEL-1173 Numerically Controlled Oscillator (NCO) and an AD9713 Digital to Analog Convertor (DAC). The NCO is controlled by the MC68332 Motorola 16 bit processor which provides 3 microhertz resolution at (Ft/17 - 110) Mhz (9.1 - 14.7 MHz). This enables the transmitter to sweep at less than 0.1 millihertz increments. The NCO output is filtered and sent to the RF board (A3B) where it is phase locked to the output of mixer U6. The 110 Mhz reference from A2 comes in at J6 on the front panel. The power divider U42 splits the reference into two paths. One path goes out J8 on the front panel where it is used in A4 the Receiver Synthesizer Module. The other path goes to the RF board A3B where it mixes with the output of VC01 the transmitter’s VCO (119.1 - 124.7 Mhz). The difference frequency (9.1 - 14.7 Mhz) is phase detected with the NCO (9.1 - 14.7 Mhz) to provide the control voltage for the VCO. The VCO output goes to U12 a three-way power splitter. One output is used in the phase lock loop. One output goes to U9 (AMP-77) where it is amplified and sent out on J7 on the front panel where it goes to the RF Distribution subsystem to generate the transmitter output signal. This signal is also coupled to U8 where it is detected as being present or not present. The third output is used to generate the translator local oscillator (XLTR LO) and the times four PN Clock. The Xmtr VCO is divided by 2 to generate the reference frequency for U20, Qualcomm’s Q3036 phase lock loop. The reference is again divided by 13 and is phase detected with the translator’s VCO, VCO2, which is 19Ft/221 divided by 38. The XLTR LO is amplified and sent out J9 on the front panel where it goes to the RF distribution subsystem. The signal is also coupled to U17 where it is detected as being present or not present. The XMTR VCO is also divided by 24 to generate

the reference frequency for U21, Qualcomm's Q3036 phase lock loop. The reference is again divided by 13 and is phase detected with the PN clock oscillator VCXO1, which is 31Ft/(24*221), which gets divided by 31. The PN clock (11.8 - 12.4 Mhz) goes to U29 an ACTEL Field Programmable Gate Array (FPGA). The FPGA generates all the codes required for NASA, NADSA, and ESA. The Inphase code (IPN) goes to J2 on the front panel where it goes to the RF distribution subsystem. The Quadrature code (QPN) goes to J3 on the front panel where it goes to the RF diatribution subsystem. The forward long code epoch (F/L EPOCH) goes out J1 on the front panel where it is used for TDRS ranging measurements.

4.4.4 Receiver Frequency Synthesizer Module (A4A4)

In the following discussion refer to Figure 4-13 and Schematic 6-xx. This subassembly generates the receiver's local oscillator (RCVR LO), the track PN local oscillator (TKPN LO), the step PN local oscillator (SPN LO), the IPN local oscillator (IPN LO), the QPN local oscillator (QPN LO) and the Long Code (LC) epoch signal. The 50 Mhz reference from the Transmitter Synthesizer Module A3 comes in at J1 on the front panel. It goes to U14 an AD9696 uktrafast TTL Comparator which is used to drive Qualcomm's Numerically Controlled Osicillator (NCO) Q2334. Direct Digital Synthesis (DDS) is a method of generating frequencies which are exact multiples of a reference frequency, in this case 50 Mhz, where the characteristics of the output signal correlate with the characteristics of the reference signal. As seen in figure TBD , frequency generation is initiated by writing a digital control word to the frequency register of the phase accumulator in the NCO, through its microprocessor interface. The frequency and phase of the output signal are controlled by the values stored in the phase accumulator's registers. The DDS works on the principle that a digitized waveform of a given frequency can be generated by accumulating phase changes at a higher frequency. Any frequency can be generated by programming the phase change within the bit resolution of the phase accumulator. A phase increment is added during each clock period of the reference. The value stored in the frequency register is added to the value stored in the phase register once during each clock period of the reference. The resulting phase value (0 to full-scale) is converted to a digitized sine wave value by the sine look up function and this digital value is output from the NCO. The digitized sine wave output from the NCO is converted to an analog waveform by an AD9713, a Digital to Analog Converter (DAC). The output of the DAC has the desired sine wave as a major component, but also includes higher frequency image components generated during the conversion of the sampled waveform. A lowpass filter (LPF) is used to reduce these image signals to the desired levels. There are two NCO's, one for the RCVR LO and one is for the PN Clock and PN LOs.

4.4.5 Receiver IF Tracking Module (A4A5)

In the following discussion refer to Figure 4-14 and Schematic 6-xx. This subassembly provides the 370 MHz IF functions of gain control (AGC), 370 MHz IF amplification, 370 MHz IF signal distribution, despreading and down conversion to two 70 MHz IF channels (the carrier loop IF and PN tracking loop IF), coherent down conversion to baseband of the two 70 MHz IF channels, anti-aliasing filters, baseband amplifiers, IF signal monitors and VME/DSP bus interface circits. The A5 module is made up of two PCB's, the IF circuitry is on a RF stripline PCB while the baseband, VME and DSP bus interface circuits are on a conventional four-layer VME (160mm x 220mm) style PCB. The RF stripline board is mounted to the VME board using stand-offs.The A5 module accepts the wideband/unleveled 370 MHz IF signal from the RF Distribution unit. This signal is leveled by the digitally controlled attenuator, which is controlled by the DSP module, amplified by three RF amplifiers, then the output is distributed to several destinations:

(1)to the A6 Demodulator module, (2)a signal level detector to detect a 370 MHz IF overload condition, (3)to a RF switch that selects various RF signals for the Spectrum Analyzer Bus, and (4)to the tracking IF's. For the tracking IF's, the 370 MHz signal is split into two paths, (1)RF carrier tracking loop IF, and (2)PN tracking loop IF. In the RF carrier tracking loop IF, the370 MHz signal is downconverted to 70 MHz by frequency mixing with a 300 MHz local oscillator (SPN-LO from Module A4) that is BPSK'd with the On-time local PN codes (selected as either I-PN codes or Q-PN codes), bandpass filtered, amplified, sampled by a directional coupler (which goes to the RF switch and provides the SPA Bus with an option), then converted to baseband providing inphase and quadrature signals to the anti-aliasing filters and DC amplifiers. The inphase and quadrature signals become the inputs to the DSP, which provides the baseband signal processing algorithms, in order to acquire the PN spreading codes and then to track the RF carrier. The conversion of the 70 MHz IF to baseband is accomplished by coherently mixing it with the 70 MHz reference frequency. A phase adjustment of the carrier loop's 70 MHz reference signal is provided for zeroing-out residule phase shifts. For the other channel, the PN tracking loop IF, the process is the same, except, (1) the 300 MHz local oscillator (TKPN-LO from Module A4) has the Early-Late local PN codes and (2) the inphase and quadrature baseband signals become the inputs of the DSP that provides the baseband signal processing algorithms to track the PN code rate. Both the VME bus and the DSP bus signals are buffered. The address lines are decoded by a programmed logic devices (PAL). The only write only register is the control to the RF switch which determines the Spectrum Analyzer's RF source. Of the two status registers, the first one (Addr = $80) contains the module ID (four MS-bits); the LO signal amplifiers (which have RF level detectors on their outputs) status. Then the second status register (Addr = $81), which is a PAL, indicates; 370 MHz IF overload state; and the failure of any of the LO signals as a single status bit. This same PAL also provides the LO signal failure bit to the A5 module front panel Fault Monitor indicator, and the 370 MHz signal overload to the front panel Signal Overload indicator. The front panel, Module Address indicator, is driven by a 'pulse stretcher' in response to the module being addressed for a read or write.

4.4.6. Data Demodulator Module (A4A6)

In the following discussion refer to Figure 4-15 and Schematic 6-xx. This subassembly provides the 370 MHz IF spead spectrum data demodulation function. The 370 MHz IF carrier is despread and down converted to two 70 MHz IF channels, the I-Channel data carrier IF and the Q-Channel data carrier IF, coherent down conversion to baseband of the two 70 MHz IF channels, baseband filtering, baseband amplification, IF signal monitoring and VME/DSP bus interface circits. The A6 module is made up of two PCB's, the IF circuitry is on a RF stripline PCB while the baseband circuits and VME bus interface circuits are on a conventional four-layer VME (160mm x 220mm) style PCB. The RF stripline board is mounted to the VME board using stand-offs. The A6 Data Demodulator module accepts the wide-band/leveled 370 MHz IF signal from the A5 - Tracking Module. This signal is split into two paths. The I-Channel data carrier IF and the Q-Channel data carrier IF. In the I-Channel data carrier IF, the 370 MHz signal is downconverted to 70 MHz by frequency mixing with a 300 MHz local oscillator (IPN-LO from Module A4) that is BPSK'd with the on-time local I-PN codes, then bandpass filtered by one of two possible bandwidths, level controlled by a digital controlled attenuator to account for the various I/Q ratio, amplified, sampled by a directional coupler (which goes to the RF switch and provides the SPA Bus with an option), converted to baseband providing inphase signals to the

digitally selected filters and DC amplifiers. This signal become the input to the Bit-Sync/Decoder Module - A8 to provide the recovered data and clock from the TDRSS I- Channel. The conversion of the 70 MHz IF to baseband is accomplished by coherently mixing it with the 70 MHz reference frequency. A user controlled phase adjustment of the I-Channel's 70 MHz reference signal is provided for zeroing-out residule phase shifts. For the other channel, the Q-Channel data carrier IF, the process is the same, except, the 300 MHz local oscillator (QPN-LO from Module A4) has the Q-PN codes and the signal becomes the input to the Bit-Sync/Decoder Module A8 to provide the recovered data and clock from the TDRSS Q-Channel. Additional non-filtered baseband outputs are provided for the STEL's PRESTO, Performance Monitoring System. One for the I-Channel data and the other for the Q-Channel data. PRESTO will observe the User Transponder R/L transmitted and received signal and measure its performance. The VME bus signals are buffered. The address lines are decoded by a programmed logic devices (PAL) to respond to the required addresses. The write-only registers provide control to, the RF monitor switch; the I and Q channel IF bandwidth; the I and Q channel's I/Q ratio attenuator; and the I and Q channel's post detection bandwidths. The dual 12-bit D/A converter provides a 0 to +10 Volt control Voltage to each the 70 MHz reference frequency phase shifters. The status register returns the, module ID (four MS-bits); the LO signal amplifiers status (which have RF level detectors on their outputs). One of the the PAL's shares its function to provide the LO signal failure bit to the A6 module front panel RF Fault Monitor indicator. The front panel, Module Address indicator, is driven by a 'pulse stretcher' in response to the module being addressed for a read or write.

4.4.7. Digital Signal Processor Module (A4A7)

In the following discussion refer to Figure 4-16 and Schematic 6-xx. This subassembly implements the algorithms for PN code acquisition and tracking, carrier acquisition and tracking, AGC, and transmitter frequency sweeps in firmware using a Texas Instruments TMS320C30 32-bit floating-point DSP chip. The module receives four baseband analog signals from the Tracking IF Module (1A2A4A5) which are each converted by a 12-bit A/D converter. The A/D converters' clock is generated by dividing the 10 MHz reference input by nine, providing the 20x clock for a sample rate of 55.56 Khz. The A/D converters are mapped to the 'C30 expansion bus, so the processor accesses the samples through a memory read. A 'C30 interrupt flag is set to notify the processor when a conversion is complete. The DSP Bus is also mapped to the 'C30 expansion bus. The DSP Bus connects the 'C30 to the NCOs, the digitally controlled attenuator (DCA), and the PN code phase stepper, all of which are on other modules. The 'C30 controls the NCOs to close the carrier loop (CLNCO), to close the PN code loop (PNNCO), and to set the receiver and transmitter center frequencies (RXNCO and TXNCO). The DCA is used for digital AGC and the PN code phase stepper is used for PN code acquisition. The DSP Bus is an eight-bit data bus while the 'C30 expansion bus is a 32-bit data bus. To allow the 'C30 to only require one write for 32-bit values to the DSP Bus, the 32-bit values are latched and clocked through the DSP Bus eight bits at a time. The DSP Bus Control Logic is composed of two programmable logic devices and a counter. The control logic determines if an 8-bit or 32-bit write is being made to the DSP Bus and then sends the appropriate bytes and addresses. The 'C30 generates a Hop Clock signal which is used to synchronously change the CLNCO and PNNCO frequencies and a Dither signal which is used by the PN Generator for PN code tracking. The 'C30 receives configuration commands from the System Controller and returns status information through the

SPU Bus. This interface is accomplished by sharing dual-port RAM (DPRAM), comprised of one master and three slave 1K x 8 DPRAM chips, between the Controller and the 'C30. The Controller accesses the DPRAM eight bits at a time, while the 'C30 accesses 32 bits at a time. A software protocol and the busy signal generated by the master DPRAM prevent any conflicts arising from both processors accessing the same memory location. An interrupt is used to signal the 'C30 when the Controller has sent new information. The 'C30 primary bus is mapped to 4K of PROM and 16K of SRAM. The firmware is stored in the PROM. The SRAM is zero wait-state and is used to optimize the processor speed. The DSP Module also includes the 12-pin header and interface for use with the 'C30 development tools.

4.4.8. Bit Sync & Viterbi Decoder Module (A4A8)

In the following discussion refer to Figure 4-17 and Schematic 6-xx. The Bit Sync and Viterbi Decoder board is a dual channel independently controlled (I and Q), signal conditioner board. Each channel has a bit synchronizer, Biphase to NRZ decoder, Viterbi decoder and differential decoder, additionally the Q channel has a rate 1/3 convolutional decoder, and De-Interleaver to work in conjunction with the convolutional decoder. The board is used to recover a clock and recondition data from the SPU Receiver Demodulator Module (A4A6) or an external source. The board has built in test points that are internally routed to a scope bus for monitoring signal quality and trouble shooting. The test points can be selected and viewed on an oscilloscope. Much of the circuitry has been compressed into Programmable Gate Arrays, including the Biphase to NRZ decoder, Diferential decoder and De-Interleaver, to reduce required space.

The I channel data is brought into the board via switch SI-1 which selects baseband (bipolar) input from the I-channel demodulator, or TTL telemetry (converted to bipolar) from the external source. This analog data is digitized (8 bits) by an analog to digital converter that feeds the I-channel bit synchronizer. The bit synchronizer's clock and three bit soft decision data output goes to the Biphase to NRZ decoder. Circuitry is provided to accept bit synchronizer or clock and data from an external source, using switch SI-2A and SI-2B, bypassing the bit synchronizer. The Bϕ-NRZ decoder converts Biphase data to NRZ, and its output is fed to the rate 1/2 convolutional decoder. The convolutional decoder accepts symbols with selectable G2 symbol inverted or normal via switch SI-4. Switch SI-3 is used to bypass the Biphase to NRZ decoder. The convolutional decoder's output goes to the Differential decoder to convert data from NRZ-M or NRZ-S to NRZ-L, the final conversion. The recovered data and clock are output to the front panel of the board through 50 Ohms drivers to coax connectors. The output to the front panel is selectable through the use of switches SI-1 through SI-6, where any function can be bypassed at any time.

The Q channel data is brought into the board via switch SQ-1 which selects baseband (bipolar) input from the Q-channel demodulator, the GN subcarrier receiver, or TTL GN telemetry (converted to bipolar), from an external source. This analog data is digitized (8 bits) by the analog to digital converter (not shown), that feeds the Q-channel bit synchronizer. The bit synchronizer's clock and three bit soft decision data output goes to the Bϕ-NRZ decoder and De-interleaver. Circuitry is provided to select bit synchronizer or clock and data from an external source, using switch SQ-2A and SQ-2B, bypassing the bit synchronizer. The Bϕ-NRZ decoder converts Biphase data to NRZ , and its output is fed to the rate 1/2 or rate 1/3 convolutional

decoder. The convolutional decoder selects an input via SQ-3 and SQ-4. The input can be De-interleaver, Bϕ-NRZ, or direct bit synchronizer output symbols. The rate 1/2 convolutional decoder selects symbols with selectable G2 symbol inverted or normal via switch SQ-4. Switch SQ-3 is used to bypass the Biphase to NRZ decoder. If De-Interleaver is selected then the De-Interleaver needs to interface with the Viterbi decoder. The Viterbi decoder will inform the De-Interleaver if it can decode the incoming symbols successfully, if it can not after a specified set of attempts then the De-Interleaver will need to dismiss to another set of delay element taps. The output of the convolutional decoder is fed to the differential decoder through switch SQ-6 to convert data from NRZ-M or NRZ-S to NRZ-L, the final conversion. The decoded data and clock are output to the front panel of the board through 50 Ohms driver to coax connectors. The output to the front panel is selectable through the use of switches SQ-1 through SQ-7, where any function can be bypassed at any time.

The Bit Synchronizer is the STEL-2110A Bit synchronizer/PSK demodulator, packaged in a 181 pin Ceramic Pin Grid Array (CPGA). It provides bit timing to control the sampling of the signal from the receiver as well as feed back signal to control the frequency of an internal Numerically Controlled Oscillator (NCO), to recover the data clock. Soft decision output data is provided to facilitate the inclusion of forward error correction, using Viterbi decoding. The bit synchronizer (clock recovery) is a digital phase locked loop, which operates by integrating the input signals over one symbol period. This is done three times in addition to the nominally “on time” integration, “quarter period early” and “quarter period late” integration are also carried out. The difference between the last two gives an indication of the timing error, since the average difference will be zero when the timing is correct. This signal is used to drive an NCO , which produces the clock signal that drives the entire circuit as well as samples the incoming signal. A lock indicator output is also derived which gives an indication of when the clock recovery circuit is within 1/4 of a symbol of optimum timing. For more details See STEL-2110A Bit Synchronizer / PSK demodulator Data sheet

The Biphase to NRZ decoder accepts 3 bit soft decision Bϕ-L, M, or S formatted symbols and converts them to NRZ data, for the Viterbi decoder. It accepts symbols and symbol clock from the bit synchronizer or an external source, divides the clock by 2 to obtain the data clock, and re-clocks the NRZ converted Biphase symbols.

The convolutional decoder used in TURFTS receiver is the QUALCOMM Q1650 K=7 multi-code Rate Viterbi Decoder, packaged in an 84 pin plastic Leadless Chip Carrier (LCC), CMOS implementation. It uses forward error correction techniques to provide higher throughput data rates with improved bit error performance. The QUALCOMM Q1650 provides both convolutional encoding and Viterbi decoding. It processes data at one of 4 code rates (1/2, 1/3, 3/4, and 7/8) (currently using rate 1/2 and 1/3 only), constraint length 7. It has built in synchronization capability and operates with either one bit hard decision or 3 bit soft decision encoded data. The chip also has built in circuitry to monitor channel bit error rate, using internal re-encode and compare circuitry. The bit error outputs of the re-encode and compare circuit can be monitored using the on chip bit error rate monitor circuit For more detailed information consult the QUALCOMM Q1650 data sheet.

The Differential decoder accepts NRZ- M or S formatted data from the convolutional decoder or an external source and converts to NRZ-L, the final receiver output. This signal is output one bit hard decision to the front panel of the board through 50 Ohms driver and coax connector. For NRZ-M differentially encoded bits are synchronously shifted (2 bits) and compared (every clock cycle). If the two bits are different then the circuit yields a high output, if they are equal then the output is a low. For NRZ-S the opposite is true, and is accomplished by inverting the output with second exclusive OR gate.

TURFTS DE-Interleaver is packaged in an 84 pin Ceramic pin Grid Array (CPGA). The digital functions have been integrated into a field programmable gate array. De-Interleaving is performed by commutating the outputs of n(30) incrementally decreased delay elements to which an interleaved sequence has been input. The slaved input and output commutators are advanced for each interleaved encoded symbol and are recycled every 30 symbols. When the De-Interleaving is synchronized to the interleaving, the output of the 116 delay element of the De-Interleaver will always be a G1 encoder symbol modulo two added to the initial cover sequence state. The cover sequence is modulo two added bit by bit to the De-Interleaved symbols to provide for perfect De-Interleaving synchronization. The sequence is a cyclical repetition of the following pattern. 00001110010001010111101101001, where the first bit is for the 116th delay element and the last is for the Zero delay element. For the initial synchronization, 30 synchronization states (a synch ambiguity of 30 symbols) exist in the De-Interleaver corresponding to 30 positions of the De-Interleaving commutators. The synch strategy consists of using the results from the Viterbi decoding metric calculations to determine when the correct synch state has been selected and the Viterbi decoder has performed long enough to determine a lock condition. If it is not locked then a new synch state must be tried until the Viterbi decoder is synchronized. This synch strategy requires a direct signal path for the metric quality between the Viterbi decoding metric calculations and the synch function associated with the De-Interleaving.

4.4.10. Data Simulator Module (A4A10)

In the following discussion refer to Figure 4-18 and Schematic 6-xx. The Data Simulator Module is a dual channel (I and Q) independently controlled signal generator board. Each channel has a bit rate generator, pseudo random code data generator, Differential encoder, convolutional encoder, NRZ to Biphase converter, and circuitry to route data to the front and rear panel of the board. In addition, the Q-channel has a rate 1/3 encoder and Interleaver. This board generates simulated telemetry data to perform loop test and bit error rate tests. The board has built-in test points internally routed to a scope bus for monitoring signal quality and trouble shooting. The test points can be selected and viewed on an oscilloscope. Much of the circuitry has been compressed into Programmable Gate Arrays to reduce space. The circuits include the convolutional encoder, NRZ to Biphase encoder, Differential encoder, and Interleaver.

The I-channel data generator gets a synthesized bit rate clock from the I-channel Direct digital synthesizer, that generates a variable digital clock rate from DC to 10Mhz. The data generator is a pseudo random code generator that generates a standard, configurable bit sequence comparable to the bit sequence generated by commercial bit error rate test machines. Its output is NRZ-L and goes to the Differential encoder to differentially format the data from NRZ-L to NRZ-M or NRZ-S. The differentially encoded data is input to the convolutional encoder to convolutional encode the data (rate 1/2). The output can have G2 symbol normal or inverted, selectable by switch SI-2.

The symbols are then formatted from NRZ-L to Bϕ-L, M, or S in the NRZ to Biphase encoder block. This is the final conversion to the signal before it sending it to the transmitter. The signal is also sent to the Q-channel switch SQ-4 as an additional option for the Q-channel transmitter and test purposes.

The Q-channel data generator gets a synthesized bit rate clock from the Q-channel Direct digital synthesizer that generates a variable digital clock rate from DC to 10Mhz. The data generator is a pseudo random code generator that generates a standard configurable bit sequence Comparable to the bit sequence generated by commercial bit error rate machines. Its output is NRZ-L and goes to the Differential encoder to differentially format NRZ-L data to NRZ-M or NRZ-S. The differentially encoded data is input to the convolutional encoder to convolutional encode the data (rate 1/2 or 1/3). The output can have G2 symbol normal or inverted, selectable by switch SQ-2 (rate 1/2 only). The output symbols can be input to either the Interleaver when using the de-Interleaver option on the receiver, or the NRZ to Biphase converter to convert NRZ-L symbols to Bϕ-L, M, or S format. Switch SQ-4 selects the final output and routes it to the transmitter, the transponder under test, or GN sub carrier module for use when TURFTS is in GN mode.

The bit rate generator is a clock signal synthesized from a 50 MHz clock using Direct digital synthesis (DDS). It can generate clock rates from DC to 10 Mhz, at 12 mhz steps. The DDS uses the QUALCOMM-Q2334, Numerically Controlled Oscillator, (NCO). The NCO is packaged in a standard 84 pin LCC, low power CMOS implementation. Direct Digital Synthesis is a method of generating frequencies that are exact multiples of a reference frequency, where the characteristics of the output signal correlate with those of the reference signal. Frequency generation is initiated by writing a digital control word to the frequency register of the phase accumulator in the NCO. The frequency and phase of the output signal are controlled by the values stored in the phase accumulator's registers. The DDS works on the principle that a digitized waveform of a given frequency can be generated by accumulating phase changes at a higher frequency. Any frequency can be generated by programming the phase change within the bit resolution of the phase accumulator. A phase increment is added during each clock period of the reference. The value stored in the frequency register is added to the value stored in the phase register once during each clock period of the reference. The resulting phase value (0 to full-scale) is converted to a digitized sine wave value by the sine look up function and this digital value is output from the NCO device. The digitized sine wave output from the NCO is converted to an analog waveform by a Digital to Analog Converter (DAC). The output of the DAC has the desired sine wave as a major component, but also includes higher frequency image components generated during the conversion of sampled waveform. A low-pass filter (LPF) is used to reduce these image signals to the desired levels.

TURFTS test data is generated by a PRN code generator that uses the shift register principle to generate a repeating pseudo random code. We use the STEL 1032 PRN coder chip. It is software configurable to generate any PRN sequence, by configuring any feedback taps from its internal shift register. For more detailed information see STEL 1032 PRN data sheet.

The Differential Encoder converts the PRN code generated (NRZ-L data) and converts to NRZ-M or NRZ-S for use with the convolutional encoder. Differentially encoding the data eliminates the ambiguity that exists in PSK demodulation, where the 1’s and 0’s may be switched. The

pattern of 1's and 0's is put in the transitions of the data rather than the level of the signal (high or low). For NRZ-M, a "1" couses a change in signal level and a "0" couses no change. For NRZ-S, a "0" couses a change in signal level and a "1" couses no change. The circuit remembers the previous bit to determine if it needs to transition or not, by exclusive ORing the incoming data bit with the previous bit.

The convolutional encoder is used for forward error correction, (FEC), in digital communications systems to provide higher throughput data rates with improved bit error performance. A convolutional code maps a number (n) of information bits into a number (m) of single bit code words, where m>n. The ratio of n/m is referenced to as the code rate. A commonly used convolutional code (rate 1/2) transforms each information bit to two code words.

The transformation from information bits to code words is accomplished by a time convolution of the information data with a finite memory windowing function, referenced to as a generating function. In the case of the rate 1/2 code, two generating functions (G0 and G1) are convolved with the information data stream. Each time a new information data bit is considered, the G0 and G1 generating functions each create an output bit or code word C0 and C1, respectively. The length of the finite memory of the generating function is the constraint length of the code (K), in our case K=7. The convolutional decoder is packaged in a field programmable gate array together with other A10 circuitry.

The NRZ-L to Biphase encoder accepts either data or symbols from the convolutional encoder and coverts the bit steam to Biphase L, M, or S. The process doubles the bit rate and increases the number of transitions on the data to make it easier for the bit synchronizer, on the receiver, to recover the clock and resolve 1's and 0's bit ambiguities (for Bϕ-M and S only). As an example Biphase-M conversion adds a transition to the data stream at the beginning of each bit and for Biphase-M another transition in the middle of the bit for a "1" and no transition for a "0" (the opposite occurs for Biphase-S). Biphase-L adds a low to high transition in the middle of the bit for a "1" and high to low transition for a "0".

TURFTS Interleaver is packaged in an 84 pin Ceramic pin Grid Array (CPGA). The digital functions are integrated into a field programmable gate array.
Interleaving is performed by commutating the outputs of n(30) incrementally increased delay elements to which the pre-interleaved sequence has been input. The slaved input and output commutators are advanced for each interleaved encoded symbol and repeat every 30 symbols. The input to the Zero delay element of the Interleaver is always a G1 encoder symbol, module-2 added to the initial cover sequence.
The cover sequence is module two added bit by bit to the pre-interleaved symbols to provide for perfect de-interleaving synchronization. The sequence is a cyclical repetition of the following pattern. 00001110010000101011110110100 1, where the first bit is for the zero delay element and the last is for the 116 delay element.
For the initial synchronization, 30 synchronization states exist in the Interleaver corresponding to 30 positions of the interleaving commutators. The cover sequence is synchronized with the interleaving delay selection so that the first bit occurs during the zero delay selection by the interleaving commutation. The convolutional encoding is synchronized with the interleaving delay

selection so that the symbol from the G1 generator of the convolutional encoding occurs during the zero delay selection by the interleaving commutation. Therefore the encoding, cover sequence generation, modulo-2 addition, and interleaving must be synchronous.

4.4.12. GN Module (A4A12)

In the following discussion refer to Figure 4-19 and Schematic 6-xx.